Notice of Allowability	Application No.	Applicant(s)	
	10/017,073	SINDHUSHAYANA ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed October 5, 2005*.

2. ☒ The allowed claim(s) is/are *1-3, 8, 13, and 25-34 renumbered as claims 1-15*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20051024* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

EXAMINER'S AMENDMENT

1. Claims 1-3, 8, 9, 13, and 25-34 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with George Pappas on October 21, 2005.

The application has been amended as follows wherein the following versions of claims 1, 25-28, and 31-34 replace all prior versions in their entirety and claim 9 is cancelled:

1. A searcher for finding the frequency of a received signal comprising a phase error, the searcher comprising:

a frequency locked loop that generates a phase increment signal in response to the phase error of the received signal;

a programmable rotator coupled to the frequency locked loop, the programmable rotator performing a phase rotation function;

a phase error accumulator accumulating results of the phase increment signals from the frequency locked loop and generating a control signal that instructs the programmable rotator to perform the phase rotation function; and

a shift register coupled between the phase error accumulator and the programmable rotator, the shift register truncating a predetermined number of bits of the control signal,

<u>wherein the frequency locked loop further comprises means for generating an initial phase signal that is coupled to the programmable rotator and initializes the programmable rotator to a predetermined starting phase</u>.

9. (CANCELLED) ~~The searcher of claim 2 wherein the frequency locked loop further comprises means for generating an initial phase signal that is coupled to the 8-Phase Shift Keying programmable rotator and initializes the 8-Phase Shift Keying programmable rotator to a predetermined starting phase.~~

25. A searcher for finding the frequency of a received signal comprising a plurality of segments, the searcher comprising:

a first phase rotator configured to phase rotate a signal to partially reduce a phase error of the signal and produce a first phase rotator output signal;

an accumulator configured to accumulate a plurality of chips from the first phase rotator output signal to form segments of the first phase rotator output signal;

a second rotator configured to phase rotate the segments of the first phase rotator output signal to further reduce ~~the~~ a phase error of the ~~signal~~ segments by adjusting the phase over each segment; and

wherein the second rotator is implemented within a frequency locked loop producing a phase increment signal based on the phase error of the segments, the first phase rotator configured to phase rotate the signal based on an accumulation of the phase increment signal.

26. A searcher in accordance with claim 25, wherein the second rotator is implemented within a frequency locked loop producing a phase increment signal based on the phase error of the segments, the first phase rotator configured to phase rotate the signal based on the phase increment signal.

27. A searcher in accordance with claim 26, wherein the first phase rotator is configured to partially reduce the phase error of the signal by compensating for instantaneous signal phase changes over each segment.

28. A searcher in accordance with claim 27, wherein the second phase rotator is configured to partially phase rotate the ~~signal~~ segments based on an average phase of the signal over multiple ~~segments~~ chips.

31. A method of finding a signal having a deviation from an expected frequency, the method comprising:

first phase rotating a signal to partially reduce a phase error of the signal and produce a partially rotated output signal;

accumulating a plurality of chips from the partially rotated output signal to form segments of the partially rotated output signal;

second phase rotating the segments of the partially rotated output signal to further reduce ~~the~~ a phase error of the ~~signal~~ segments by adjusting the phase over each segment; and

generating a phase increment signal based on the phase error of the segments, the first phase rotating the signal to partially reduce the phase error of the signal based on an accumulation of the phase increment signal.

32. A method in accordance with claim 31, further comprising:

generating a phase increment signal based on the phase error of the segments, the first phase rotating the signal to partially reduce the phase error of the signal based on the phase increment signal.

33. A method in accordance with claim 32, wherein the first phase rotating the signal to partially reduce the phase error of the signal comprises compensating for instantaneous signal phase changes over each segment.

34. A method in accordance with claim 33, wherein the second phase rotating the signal to further reduce the phase error of the segments comprises compensating for instantaneous signal phase changes over each segment by partially phase rotating the signal based on an average phase of the signal over multiple ~~segments~~ chips.

Claims 31-34 are renumbered as claims 1-4, claims 25-30 are renumbered as claims 5-10, claims 1-3, 8, and 13 are renumbered as claims 11-15, and the claim dependency is renumbered accordingly.

Allowable Subject Matter

3. Claims 1-3, 8, 13, and 25-34 renumbered as claims 1-15 are allowed.

4. The following is an examiner's statement of reasons for allowance:

Claims 1-3, 8, 13, and 25-34 renumbered as claims 1-15 are allowed because the prior art of record does not disclose or obviate any of the independent claims 1, 25, or 31. That is, the prior art of record does not disclose a frequency locked loop as claimed in claim 1 having a means for generating an initial phase signal and a shift register coupled between the phase error accumulator and the programmable rotator. Regarding independent claims 25 and 34, the prior art of record does not disclose or obviate a frequency locked loop having accumulators preceding both a first and a second phase rotator as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
October 24, 2005

jmp